AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims

1. (Currently Amended) An Active load arrangement (Z) for providing output DC load to an object (TO) under AC test, the arrangement (Z) including a voltage controlled transistor (MOSFET) having a source (S), a gate (G) and a drain (D), wherein the drain (D) is associated with the gate (G) and connected to an arrangement input (I2) associated with the object (TO), and the source (S) is connected to an arrangement output (O2) associated with the object, the active load arrangement further comprising:

a feedback arrangement connected to the source (S) and to the gate (G), for obtaining low impedance at low frequencies and high impedance at high frequencies by ~~the feedback arrangement varying frequency changes,~~ varying phase and amplitude of the gate-to-source voltage in accordance with variations in frequency, said feedback arrangement comprising:

a first feedback net (FBN1) in which an inductance (L1) is connected between the source (S) and the arrangement output (O2); and

a second feedback net (FBN2) in which a first resistance (R1) is connected between the gate (G) and the arrangement input (I2), and a second resistance (R2) is connected between the gate (G) and the source (S), and a capacitor (C1) is connected between the gate (G) and the arrangement output (O2).

2-3. (Canceled)

4. (Previously Presented) An active load arrangement (Z) for providing proper DC output load to an object (TO) under AC test, the arrangement (Z) comprising a voltage controlled transistor (MOSFET) having a source (S), a gate (G) and a drain (D), the drain being connected to an arrangement input (I2) associated with an output (O1) of

the object (TO), whereby a first resistance (R1) is connected between the gate (G) and the drain (D), the active load arrangement further comprising:

an inductance (L1) being connected between the source (S) and an arrangement output (O2) associated with an input (I1) of the object (TO), and a capacitance (C1) being connected between the gate (G) and the arrangement output (O2).

5. (Previously Presented) The active load arrangement (Z) according to claim 4, whereby a second resistance (R2) is connected between the gate (G) and the source (S).

6. (Previously Presented) The active load arrangement (Z) according to claim 4, whereby a second resistance (R2) is connected in parallel with the capacitance (C1).

7. (Previously Presented) The active load arrangement (Z) according to claim 4, whereby a rectifier bridge is connected between the test object (TO) and the test arrangement (TA).

8. (Currently Amended) An active load arrangement (Z1) for providing output load to an object (TO) under test, comprising:

~~a second active load arrangement comprising:~~

a first voltage controlled transistor (MOSFET) having a source (S), a gate (G) and a drain (D), wherein the drain (D) is associated with the gate (G) and connected to an arrangement input (I2) associated with the object (TO), and the source (S) is connected to an arrangement output (O2) associated with the object, the ~~second~~ active load arrangement further comprising a feedback arrangement connected to the source (S) and to the gate (G), for obtaining low impedance at low frequencies and high impedance at high frequencies by ~~the feedback arrangement varying frequency changes,~~ varying phase and amplitude of the gate-to-source voltage in accordance with variations in frequency; and

a second voltage controlled transistor (MOSFET2) ~~comprising~~ having a second source (S2), a second gate (G2) and a second drain (D2), the second source (S2) being connected via the feedback arrangement to the source (S) and the gate (G) via a third resistor (R4) and a first capacitor (C1) to the second gate (G2), the second gate (G2) being connected via a fourth resistance (R5) to the drain (D2) and to an arrangement output (O3) associated with the test object (TO) and the second gate (G2) being connected to the source (S) via a second capacitor (C2).

9. (Previously Presented) The active load arrangement (Z1) according to claim 8, wherein the feedback arrangement comprises a first feedback net (FBN1) in which an inductance (L1) is connected between the source (S) and the arrangement output (O2).

10. (Previously Presented) The active load arrangement (Z1) according to claim 9, wherein the feedback arrangement further comprises a second feedback net (FBN2) in which a first resistance (R1) is connected between the gate (G) and the arrangement input (I2), and a second resistance (R2) is connected between the gate (G) and the source (S), and a capacitor (C1) is connected between the gate (G) and the arrangement output (O2).